Semi-analytical modeling of high performance nano-scale complementary logic gates utilizing ballistic carbon nanotube transistors

Mohammad Khaleqi Qaleh Jooq\textsuperscript{a}, Ali Mir\textsuperscript{b,∗}, Satar Mirzakuchaki\textsuperscript{b}, Ali Farmani\textsuperscript{a}

\textsuperscript{a} Department of Electrical Engineering, Lorestan University, Lorestan, Khorramabad, Iran
\textsuperscript{b} Electrical Engineering Department of Iran University of Science and Technology, Narmak, Tehran, Iran

Abstract
Carbon nanotube field effect transistors (CNTFETs) have gained remarkable attention in modern fields, as one of the promising candidates for replacing conventional MOSFETs technology at the end of the roadmap. In this regard, this article presents high-performance complementary logic gates based on ballistic gate-all-around CNTFETs utilizing a novel improved analytical model. This is done by considering the effects of carrier density, quantum capacitance, and the number of channels, which are highly suitable for logic applications. For this purpose, the polarities of CNTFETs are switched between n- and p-type by harnessing its geometrical properties (i.e. the dielectric materials). In the present paper the semi-analytical method is utilized to design complementary logic gates including inverter, AND, and XOR. To benchmark the structure, the main parameters including propagation delay, power delay product, noise margin, and static and dynamic power consumptions are calculated. Then appropriate values are achieved and then used in a simple half adder. It is shown that by applying a small external voltage in the order of 0.8 \textit{V}, the enhanced design metrics including static and dynamic powers can be achieved as $P_S = 25.12 \text{ pW}$, and $P_D = 40.62 \text{ nW}$ respectively. To verify the obtained results, they are compared with those of numerical and experimental models. Our results highlight the use of complementary gate-all-around CNTFET transistors as a promising platform for computing applications.

1. Introduction

Logic gates have been in the spotlight in modern fields including bio-computing systems [1], nanostructure computers [2], quantum computing systems [3,4], photonic technologies [5–8], and modern medicine [9], and have become a hotspot in both empirical and scholarly types of research. For high performance logic applications, the topmost desired features of logic gates are: small footprint, high gain, small footprint, high gain, and high $I_{on}/I_{off}$ ratio. Low power consumption is another pivotal parameter in logic devices which corresponds to a low applied voltage [10–12]. To realize of logic gates with appropriate properties, various schemes have been proposed so far such as all metallic structures [13], molecular structures [14], spin-based structures [15], and nanowire heterostructures [16]. Many of these structures operate via two mechanisms including electron injection into ferromagnetic metals and spin injection to semiconductors. However, most of these platforms suffer from several inherent limitations, namely long channel length, the Schottky barrier, and scattering from charged dopants which restrict the performance and mobility of these devices. For instance, silicon-germanium nanowire heterostructure-based transistors usually have a non-ballistic behaviour which limits the performance of the device [16]. From a practical perspective, these structures suffer from the a serious problem, i.e. their large channel length which leads to high scattering.

To address the abovementioned concerns, advanced materials such as 2D materials such as transition metal dichalcogenide (TMD) and carbon allotropes such as graphene are a potential candidates to design the field effect transistors. TMDs with having different 40 families, especially semiconductor Molybdenum disulfide (MoS\textsubscript{2}) monolayer with 1.8 eV direct band gap, extraordinary $I_{on}/I_{off}$ current ratio at room temperature, appropriate mobility, good mechanical strength and flexibility, has received a much attention of the nanoelectronics Scientists. However, despite of these prominent properties of TMD materials, increasing the contact resistance of the TMD-metal interface plays a pivotal role and restrain the performance of the device. This limitation is mainly due to the creation of the additional tunneling barrier along with the inherent Schottky barrier caused by van-der-Waals gap at the interface. Therefore, resulted tunneling barrier restricts the performance of the devices and more complex contact methods (such as metalizing the channel under the contact metal) is...
needed for harnessing the full potential of the TMD based devices [17–20].

By introducing the types of carbon forms as a channels in transistors, the carrier can be confined into a subwavelength-scale region which provides compact integrated circuit [21–28]. Moreover, the scattering and the length of the channel are decreased. Hence, the high performance logic gates is ensured. Amongst carbon allotropes, carbon nanotubes (CNTs) have recently attracted a lot of attention due to their three main extraordinary properties [29–33] including: (i) their pristine one-dimensional structure making them ideally suited for nano-scale logic gates in which the scattering probability is remarkably reduced, therefore, the carbon nanotube-based transistors can operate in ballistic regime [34,35], (ii) the Schottky barrier between a carbon nanotube and metal contacts which can be utilized for logic gates [36], and (iii): the electronic properties of a carbon nanotube which can be easily manipulated through its chemical doping in contrast to previous platforms. It is worth to mention that, the obtained Schottky barrier at the semiconductor-metal interface which restricts the performance of the nearly all nanotransistors can be eliminated by using carbon allotropes (e.g. semimetal graphene) as the metal contact to the CNT for both n-type and p-type devices.

Despite these worthwhile properties, the conventional carbon nanotube can usually be used as a p-type channel (owing to moisture), while to realize complementary architectures which are power efficient circuits for logic applications, the n-type channel is also needed [37]. To solve this issue, various approaches have been introduced and utilized such as applying different chemical potentials [38], the application of metal contacts with different work functions [39], and using different gate dielectrics [40].

It is worth mentioning that two main categories of carbon nanotube-based transistors have been noted in the literature as the planar-type structures (suitable for on-chip applications) [41,42] and the gate all around-type structures (suitable for off-chip applications) [43–45] which use the abovementioned approaches to achieve logic gates with a complementary architecture. For example, Raj’s research group proposed several ultra-low power memories based on logic gates using carbon nanotube transistors [42,43]. Analogously, Franklin’s research group theoretically and experimentally reported high performance logic gates utilizing carbon nanotube transistors [44,45]. From the theoretical and practical perspectives, some of these structures with a large channel length, relative high static power, and low current ratio are not suitable for nanostructure logic applications.

To cope with this issue, several structures have been proposed with exact experimental and theoretical analyses. Therefore, many authors have used various numerical and experimental analyses to present carbon nanotube-based transistors which suitable for logic applications [46].

In our previous works, we numerically focused on the performance dependency of a ballistic carbon nanotube transistor by harnessing the applied doping and gate dielectric thickness [47–49]. Here, we design new ballistic carbon nanotube logic gates including an inverter, AND, and XOR, and use the rigorous and effective semi-analytical method to analyze the structure. In addition, the effects of chemical doping and geometrical parameters on the operation of the device are investigated. Furthermore, to enhance the performance of logic gates including gain, static power, and dynamic power, the effect of arrays of carbon nanotube as a channel is investigated and utilized to implement a simple 1-bit half adder. In this platform, by properly adjusting the chemical potential through applied voltage on a carbon nanotube, high performance complementary logic gates can be realized. The analytical simulation results show that compared with previous works both the $I_{\text{on}}/I_{\text{off}}$ ratio and gain are relatively enhanced, whereas the power delay product (PDP), and static and dynamic power consumptions are decreased considerably. The performance parameters for logic gates are provided in what follows. The main parameters for the standard inverter are $P_{d} = 33.1 \text{nW}$, $P_{p} = 159 \text{nW}$, $t_{d} = 12 \mu\text{s}$, $PDP = 1.908 \text{pJ}$, and $\text{gain} = 3.75 \text{V/V}$. The metrics for standard AND logic gate have been calculated as: $P_{d} = 52.5 \text{nW}$, $P_{p} = 32.9 \mu\text{W}$, $t_{d} = 25.1 \mu\text{s}$, and $PDP = 0.82 \text{nJ}$. The metrics for standard XOR logic gate are: $P_{d} = 99.1 \text{nW}$, $P_{p} = 98.7 \mu\text{W}$, $t_{d} = 602.3 \mu\text{s}$, and $PDP = 59.44 \text{nJ}$.

By harnessing the nanotube diameter, and increasing the number of channels, the performance of the parameters is notably improved. For this purpose, we have demonstrated a 1-bit half adder and have investigated the impact of the abovementioned parameters on the performance of the proposed model. The results presented here demonstrate that by applying a small external voltages in the order of 0.8 V, enhanced design metrics including static and dynamic powers can be achieved as $P_{d} = 25.12 \text{pW}$, and $P_{p} = 40.62 \text{nW}$, respectively. We believe that the presented model can have potential applications in nanoscale logic devices and is suitable for practical applications.

The rest of this paper is organized as follows. In Section 2, the structure of the proposed gate-all-around logic gate is presented. Then, the carrier density, quantum capacitor, and surface potential of the structure are calculated. For this purpose, the electronic properties of the carbon nanotube are reviewed and further investigated through an analytical simulation. In the same section, it is shown that by applying a variable external voltage, the chemical doping of the carbon nanotube can be shifted above or below the threshold value and as a result its electronic properties can be manipulated. In Section 3, by utilizing an analytical method and considering proper conditions, we investigate and discuss the dependencies of the logic gate operation on the geometric parameters including arrays of channels and CNT’s diameter. Also briefly and comprehensively, the main parameters of the improved complementary logic gate are discussed and compared with previous works in this Section. Finally, we summarize the main conclusions in Section 4.

2. Model and theory

2.1. The proposed CNTFET transistor

As mentioned in the previous section, carbon nanotube-based transistors are divided into two categories: planar and gate-all-around platforms. Planar FETs have been the core of VLSI circuits for many decades [50]. However, as the length of the channel decreases, planar platforms suffer from the undesirable short channel effects (SCE), especially the high leakage current which leads to a high power consumption in the off-state regime [51–53]. To overcome this obstacle, the gate-all-around (GAA) configuration has been introduced here. The outstanding properties of the earlier configuration including low leakage current, higher $I_{\text{on}}/I_{\text{off}}$ current ratio and improved carrier transport open a new way to sub-scale systems [54,55]. In addition, GAA CNTFETs have remarkably improve the electrostatic control over the channels encapsulated by wrap gate and provide extraordinary performance owing to considerable SCE as compared with their planar counterparts. Besides, their drain-induced barrier lowering (DIBL) hampering, and fascinating subthreshold slope (SS) highlight the advantages of GAA CNTFET devices [44,45].

The proposed ballistic GAA CNTFET with a 20 nm channel length has been shown in Fig. 1. To restrict the threshold voltage alternation, a 1 nm AlO$_{x}$/N$_{x}$ adhesion layer is applied. This layer also eliminates the hysteresis and, therefore, improves the SS. To suppress the return-back leakage current, high-k dielectric materials (8 nm HfO$_{2}$ for n- and 8 nm Al$_{2}$O$_{3}$ for p-type) are deposited around the nanotube and are suspended on a silicon–on–insulator substrate. A spacer which refers to the distance between the gate and the source/drain contacts (i.e. $L_{\text{sp}}$) plays a crucial role in the performance of the device. The application of spacer restricts the ambipolar conduction, because it provides a barrier against carrier transport in the devices which are not modulated by the gate. Although the spacer regions are not doped in p-type structures, parasitic resistances affect the drive current which should be taken into account in modeling the device. To provide a gate metal that
completely surrounds the channel, a 5 nm-thick TaN gate contact is used. It is worth mentioning that by utilizing appropriate gate dielectric and chemical doping, the polarity of the device can be harnessed. Hence, complementary (n- and p-type) devices can be provided. In what follows, the carrier density, quantum capacitance, and surface potential are reviewed and then calculated as the main parameters of the GAA CNTFET.

2.2. The calculation of Carrier density and quantum capacitance

In this section, the carrier density as transport properties of the GAA CNTFET is investigated. Carrier density, which has been considered for the charges in the channel, is calculated by the density of states (DOS(E)) with probability function which is expressed as [56]:

\[
\int_{-\infty}^{\infty} n \text{DOS}(E) f(E) dE = \frac{A_1 D_0}{\sqrt{E - E_{CB}}} + A_2 D_0 H(E - E_{CB})
\]

(3)

where \(E_{CB} = \phi_s - E_f/2\) is the bottom energy value of the first sub-band (\(\phi_s\) denotes the channel surface potential and \(E_f\) is the bandgap energy) and \(D_0 \approx 2 \text{nm}^{-1} \text{eV}^{-1}\) is the metallic DOS [58]. Unfortunately, using Eq. (2) in carrier density integral cannot lead to an analytical closed-form solution. However, under some assumptions, an analytical approximation may be achieved. From Eq. (2), for \(E \ll \gamma\) (where \(\gamma\) is the tight binding energy, \(\gamma = 3.1\ \text{eV}\)) DOS(E) exhibits the inverse square-root dependence \(\text{DOS}(E) \sim 1/\sqrt{E}\), while at energies above the \(E_{CB}\), it approaches a constant value of \(D_0/2\). Based on this viewpoint, we have proposed the following semi-analytical formula:

\[
\text{DOS}(E) \approx \frac{A_1 D_0}{\sqrt{E - E_{CB}}} + A_2 D_0 H(E - E_{CB})
\]

(3)

where \(H\) denotes the Heaviside function and \(A_1\) and \(A_2\) can be expressed empirically as the polynomials of \(E_f\) as:

\[
A_1 = -0.034E_f^2 + 0.152E_f + 0.0465
A_2 = -0.126E_f^2 + 0.462E_f + 0.019
\]

(4)

Fig. 2 shows a comparison among the first sub-bands of the universal DOS [57], the semiconductor polyynic carbyne DOS, the nanowire DOS [59] and the proposed semi-analytical DOS. It can easily be seen that, at higher energies, the nanowire DOS tends to zero. Therefore, the nanowire DOS approximation underestimates the carbon nanotube DOS for energies above \(E_f\). It can be seen that the proposed DOS is valid for polyynic carbyne at lower energies \((E < < \gamma)\). Moreover, it is worth mentioning that due to the very short length of these materials, complex quantum behaviors such as direct source to drain tunneling will become significant. Since our model ignored these complex quantum mechanical effects, therefore is not being capable to capture the I-V characteristics of polyynic carbynes. By substituting Eq. (3) in Eq. (1), the carrier density is obtained as:

\[
n = n_s + n_b = \int_{E_{CB}}^{\infty} \left( \frac{A_1 D_0}{1 + \exp \left( \frac{E - E_f}{k_B T} \right)} \right) dE + \int_{E_{CB}}^{\infty} A_2 D_0 H(E - E_{CB}) dE
\]

(5)

Fig. 2. Comparison among the first sub-bands of the universal DOS, the semiconductor polyynic carbyne DOS, the nanowire DOS, and the proposed semi-analytical DOS.